NanoCell

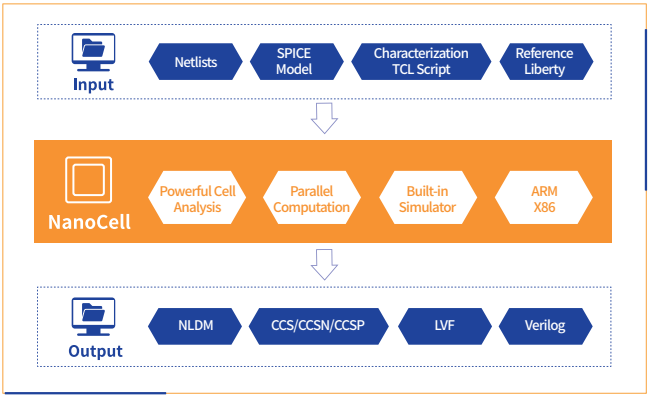
PRIMARIUS

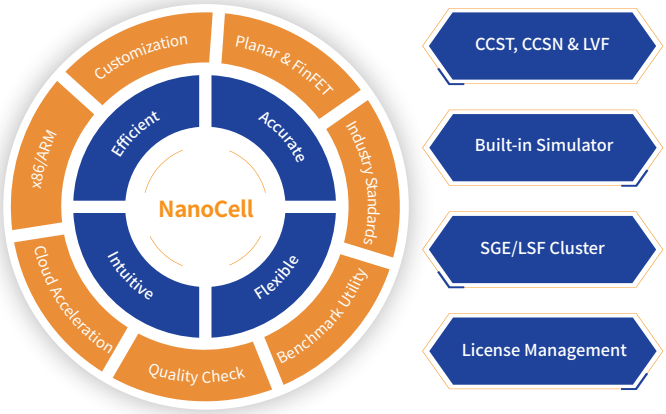
Standard Cell Library Characterization Solution

Introduction

A standard cell library is essential for chip design, including circuit design, layout design, and characterization. The standard cell library characterization needs many simulations, model extraction, and verification, which occupies more than one-third of the time in developing a standard cell library. Therefore, improving the efficiency of the standard cell library characterization is the key to shortening the development cycle. With the shrinking of process nodes, the design complexity of the chip increases day by day. Under the advanced technology, the introduction of many signoff process corners and the ultra-low voltage design of near-threshold voltage put forward higher requirements for the feature extraction of cell libraries, such as timing, power consumption, noise, and statistical variation. So, the amount of simulation calculation increases exponentially, which has become the bottleneck of digital chip design.

NanoCell is a fast, accurate, and easy-to-use standard cell library characterization EDA tool. It adopts intelligent analysis algorithms to analyze and extract arcs and functionalities of the cells. By leveraging advanced distributed computation technology and a powerful built-in NanoSpice engine, it accurately and efficiently simulates and builds the timing, power consumption, noise, and other characteristics of standard cells, supporting planar and FinFET process (advanced node down to 7nm). Also, NanoCell provides user-friendly and easy-to-use interfaces to help users shorten product development cycles.





Specifications

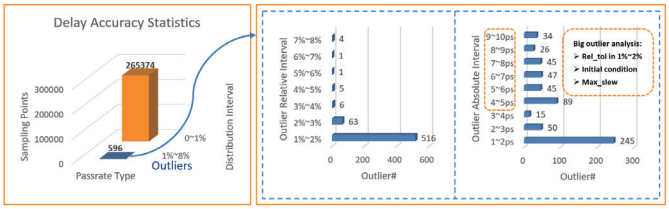
- SGE and LSF cluster support
- ARM/X86 environment enablement
- Local and distributed multi-process support
- Built-in and external simulator enablement
- New-Lib Characterization/Re-Characterization
- NLDM/CCS/CCSN/CCSP/Moment-based LVF model
- Combinational/Sequential/Special cell characterization
- Aligning with benchmark tools

Applications

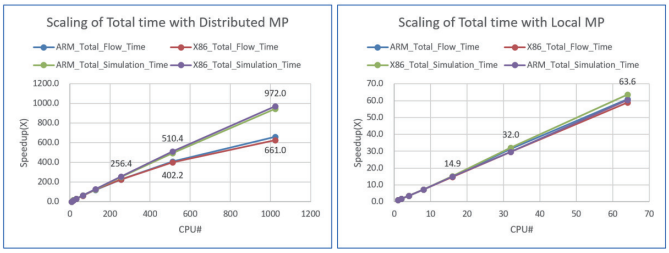
- Foundry Library Characterization & Re-Characterization
- IP Vendor Library Characterization & Re-Characterization
- Fabless companies Library Characterization & Re-Characterization

Application Examples

Delay Accuracy Pass Rate Distribution Figure



Total Simulation Time Linear Scaling in Local and Distributed MP



Key Advantages

- Fast
  2X faster than REF tool with advanced distributed parallel architecture
- Flexible
  Powerful cell circuit analysis algorithm, complete ARC extraction
- High-precision
  Built-in NanoSpice & advanced library characterization models support
- Easy-to-use
  Simplified user interface and configuration with built-in benchmark liberty utility
- Multi-platform
  ARM/X86 environment & SGE/LSF cluster support with good scaling