NanoSpice Pro

PRIMARIUS

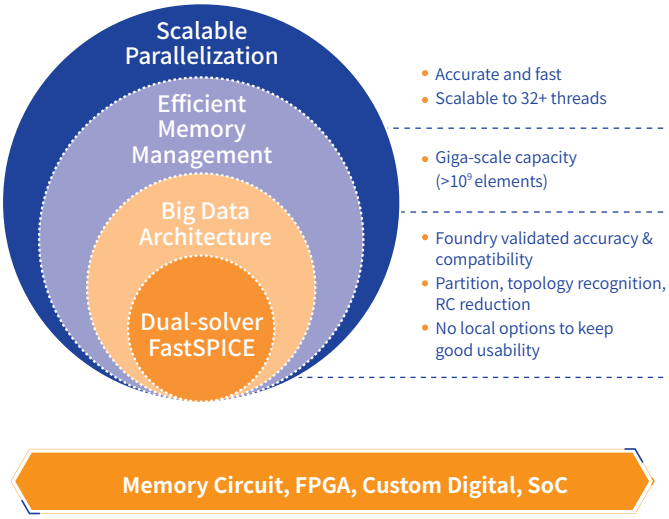
High Performance FastSPICE Simulator

Introduction

NanoSpice Pro is a revolutionary high-performance and high-capacity FastSPICE circuit simulator. Its dual-solver engine boosts the simulation throughput of all modern complex designs, including memory (DRAM, SRAM, Flash, MRAM), FPGA, custom digital, and SoC circuits.

With the breakthrough FastSPICE algorithm, intelligent topology recognition, and automatic partition technology, NanoSpice Pro delivers superior performance and capacity to address advanced node verification challenges. Adaptive dual-solver technology, i.e., seamless integration of the state-of-the-art digital engine and the giga-scale analog engine, ensures superior analog accuracy and digital performance for mixed-signal designs.

NanoSpice Pro provides a unique one-stop memory simulation solution to meet all needs for memory cell design, memory array and compiler verification, memory characterization, and full-chip verification with up to 10X+ performance increase over other commercial simulators.



Key Advantages

- Breakthrough algorithm
  Intelligent topology recognition and automatic partitioning
- Higher capacity
  Up to 10X+ faster simulation throughput
- Advanced RC reduction and fast yet accurate model evaluation
- Adaptive dual-solver
  Superior analog accuracy and digital performance
- High Performance
  Performance scales linearly with 32+ multi-core simulations
- Unique one-stop memory simulation solution

Application Examples

Full-chip Circuit Type	Reference	NanoSpice Pro	Speedup
DRAM	25.2 days	3.9 days	6.5 X
SRAM	35.5 hours	4.2 hours	8.5 X
Flash	6.6 days	1.6 days	4.1 X

Specifications

- Supports HSPICE and Spectre netlist formats
- Supports all public domain models, user-defined models
  - MOSFET: BSIM3, BSIM4, BSIM-BULK, BSIM-IMG, BSIM-CMG, BSIM-SOI, LETI-UTSOI, PSP, HiSIM2, HiSIM_HV, EKV3
  - BJT: MAXTRAM, VBIC, HICUM; TFT: a-Si TFT, poly-Si TFT
  - Diode: JUNCAP, JUNCAP200, DIODE_CMC; Varactor: MOSVAR
  - Resistor: R2_CMC, R3_CMC; HEMT: ASM-HEMT; JFET/MESFET; TMI; Custom PMI; Bsource
- Supports S-parameter, Transmission line (W-element, T-element), IBIS model
- Supports standard output formats for data analysis: FSDB, PSFASCII, SPICEASCII, ASCII, etc
- Unique transient output format - NWF, reduce 2x+ file size
- Supports VEC and VCD stimulus files
- Supports SPEF, DSPF, DPF back-annotation
- Supports Verilog co-simulation
- Supports public/hybrid cloud, computer farm

Applications

- Memory characterization and function verification
- SoC full-chip fast timing and functional verification
- Memory IC dynamic power dissipation and timing simulation